REMARKS

Claims 1 through 17 are pending in this patent application. Applicants would like to thank the Examiner for her careful analysis and detail comments on the claims in this application. Claims 1, 4, 12, 15, and 17 have been amended. Claim 3, 6-11, and 14 have been cancelled.

Claim Objections

Claims 1, 3, 4, 6, 7, 8, and 12 are objected for various informalities. Applicants have edited these claims to overcome the reasons stated in the office action.

Claim Rejections under 35 USC §112

Claims 1-4, 6, 8, 10, 12, 14, 16, 18, 20, and 22-25 are rejected under 35 U.S. C. §112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject mater which applicant regards as the invention.

Inventorship

The joint inventors for the pending Claims 1 through 17 remain the same.

Claim Rejections under 35 U.S.C. §103

Claims 1, 2, 5-13, and 16 are rejected under 35 U.S.C. §103 as being unpatentable over Dunlop, et al. (Dunlop) U.S. Patent 4,577,276. The Examiner stated, in pertinent part, that

> Dunlop discloses a technique for the placement of components on a circuit substrate. Dunlop does not explicitly teach a datapath structure. Rather,

Dunlop discloses the applicability of the technique to digital logic, semiconductor memories, register banks, and further to any integrated circuit chip or subchip having interconnected circuit modules (Dunlop, col. 3, II. 45-51). A datapath structure has interconnected circuit modules and has an iterative structure (reference U.S. Patent 5,726,902 to Mahmood et al., which illustrates a datapath structure features and is relied on here for referential purposes only as there would be no reason to combine this reference with Dunlop '276). Bases on the above reasoning that comes from the Dunlop disclosure, it would have been obvious to one of ordinary skill in the art that Dunlop method of cell placement is also applicable to datapath structures.

With respect to Claim 1, the Examiner stated that

Pursuant to claim 1 which recites [a] data structure (col. 3, II. 33-51), comprising one or more cell instances (modules at column 3 II. 33-51), each cell instances having a pin (terminals, col. 4, II. 23-30); one or more pseudo cell instances (pseudo modules, col. 5, II. 3-17), each pseudo cell instance in the one or more pseudo cell instances being placed at a location relative to the one or more cell instances in encouraging a predetermined structure (col. 5, II. 3-17 discloses the biasing of a partitioning structure); and one or more pseudo nets (signal nets col. 5, II. 3-18), a first pseudo net connecting between a pin of a first cell instance in the one or more cell instances and a pin in a first pseudo cell instance in the one or more pseudo cell instances (see Figure 4; col. 5, II. 35-47; col. 6, II. 1-10).

Claim 1 has been amended to recite a datapath structure, comprising:

one or more cell instances, each cell instance having a pin;

one or more pseudo cell instances, each pseudo cell instance having a pseudo pin, each pseudo cell instance in the one or more pseudo cell instances being placed at a location relative to the one or more cell instances in encouraging a predetermined structure; and

one or more pseudo nets, a first pseudo net connecting between a pin of a first cell instance in the one or more cell instances and a pin [in a pin] in a first pseudo cell instance in the one or more pseudo cell instances, wherein the <u>first pseudo cell instance being placed at a relative location to the first real cell instance</u> <u>produces a zero length in the first pseudo net</u>. (Emphasis Added).

Applicants have amended Claim 1 as suggested by the Examiner to incorporate the limitation from Claim 3 into Claim 1. Claim 3 is now cancelled. The Examiner

indicated that the prior art does not disclose producing a zero length in the first pseudo net or a pseudo length having a value greater than a zero. It is respectfully submitted that Claim 1, as amended, is patentable over the cited reference of Dunlop et al.

With respect to Claim 2, the Examiner stated that "[[p]]ursuant to claim 2, further comprising a first relative position between the first cell instance (Fig. 3, 27) and the first pseudo cell instance (Fig. 3, 28)." Claim 2 depends on Claim 1 and is patentable over the cited reference for at least the same reasons as described for Claim 1.

Claim 3 has been cancelled.

Claim 4 has been amended to incorporate the limitations in Claim 1. Claim 4 has been rewritten in independent form including the limitations of the base claim, as suggested by the Examiner.

With respect to Claim 5, the Examiner stated that "[[p]]ursuant to claim 5, wherein the predetermined structure comprises a column structure, a row structure, or a square structure (col. 6, II. 24-51 discloses a row or columnar (vertical) structure and col. 6, II. 45-49 discloses adjusting row lengths to other desired configuration which would necessarily include square structures)." Claim 5 depends on Claim 1 and is patentable over the cited reference for at least the same reasons as described for Claim 1.

Claims 6-11 have been cancelled.

With respect to Claim 12, the Examiner stated that "[[p]]ursuant to claim 12 which recites [[a]] computerized method (use of programming, col. 2, II. 40-44; col. 6, line 52 to col. 7, line 440 for encouraging a structure bonding comprising placing a first pseudo cell instance (pseudo modules, col. 5, II. 3-17) at a location relative to a first pseudo cell instance (pseudo modules, col. 5, II. 3-17) at a location relative to a first cell

instance in a plurality of cell instances for encouraging a predetermined structure (col. 5, II. 3-17 discloses the biasing of a partitioning structure) bonding in the plurality of cell instances; and connecting the pseudo net (signal nets col. 5, II. 3-18) between the cell instance and the pseudo cell instance (see Figure 4; col. 5, II. 35-47; col. 6, II. 1-10)." Claim 12 has been amended to incorporate the limitation from Claim 14, which the Examiner has indicated that it is allowable.

With respect to Claim 13, the Examiner stated that "[[p]]ursuant to claim 13, further comprising the step of minimizing a wire length in the pseudo net from the placement of the first pseudo cell instance relative to the first cell instance (col. 6, II. 11-29)."

Claim 14 has been cancelled.

Claim 15 has been rewritten in independent form including all of the limitations of the base claim.

With respect to Claim 16, the Examiner stated that "[[p]]ursuant to claim 16, wherein the predetermined structure comprises a column structure, a row structure, or a square (col. 6, II. 24-51 discloses a row or columnar (vertical) structure and col. 6, II. 45-49 discloses adjusting row lengths to other desired configuration which would necessarily include square structures." Claim 15 has been rewritten in independent form including all of the limitations of the base claim.

CONCLUSION

Claims 1-2, 4-5, 12-13, and 15-17 are pending in this application. In view of the above, it is respectfully submitted by Applicant that the claims are in condition for allowance. Reconsideration of the rejections is requested. Allowance of the claims at an early date is solicited. Formal drawings will be submitted by Applicants upon indication of allowed claims. If the Examiner's action is other than allowance, the Examiner is invited to telephone Applicants' attorney at the number noted below.

Respectfully submitted,

Peter C. Su
Attorney for Applicants
Reg. No. 43,939

Date: 7/28/2003

Address: Fernandez & Associates, LLP
Patent Attorneys
1047 El Camino Real
Menlo Park, CA 94025

Phone: (650) 325-4999
Fax: (650) 325-1203
Email: *iploft@iploft.com*